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Bangsaruntip et al.

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(54) **NANOWIRE PIN TUNNEL FIELD EFFECT DEVICES**

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(51) **Int. Cl.**

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H01L 21/04	(2006.01)
B82Y 10/00	(2011.01)
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H01L 29/423	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 21/047*** (2013.01); ***B82Y 10/00*** (2013.01); ***H01L 29/0665*** (2013.01); ***H01L 29/0669*** (2013.01); ***H01L 29/42312*** (2013.01); ***H01L 29/66356*** (2013.01); ***H01L 29/7391*** (2013.01)

(58) **Field of Classification Search**

CPC .. B82Y 10/00; H01L 21/047; H01L 29/0665; H01L 29/42312; H01L 29/0669; H01L 29/7391; H01L 29/66356

USPC 257/38

See application file for complete search history.

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Assistant Examiner — Evren Seven
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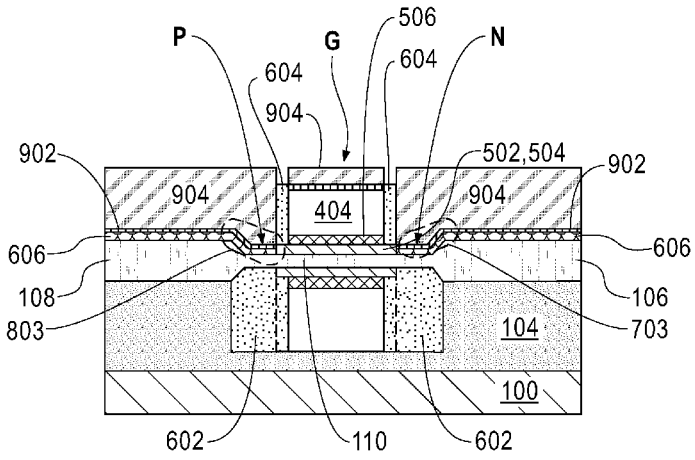
(57) **ABSTRACT**

A nanowire tunnel device includes a nanowire suspended above a semiconductor substrate by a first pad region and a second pad region, the nanowire having a channel portion surrounded by a gate structure disposed circumferentially around the nanowire, an n-type doped region including a first portion of the nanowire adjacent to the channel portion, and a p-type doped region including a second portion of the nanowire adjacent to the channel portion.

20 Claims, 5 Drawing Sheets



(51) **Int. Cl.**

H01L 29/66	(2006.01)
H01L 29/739	(2006.01)

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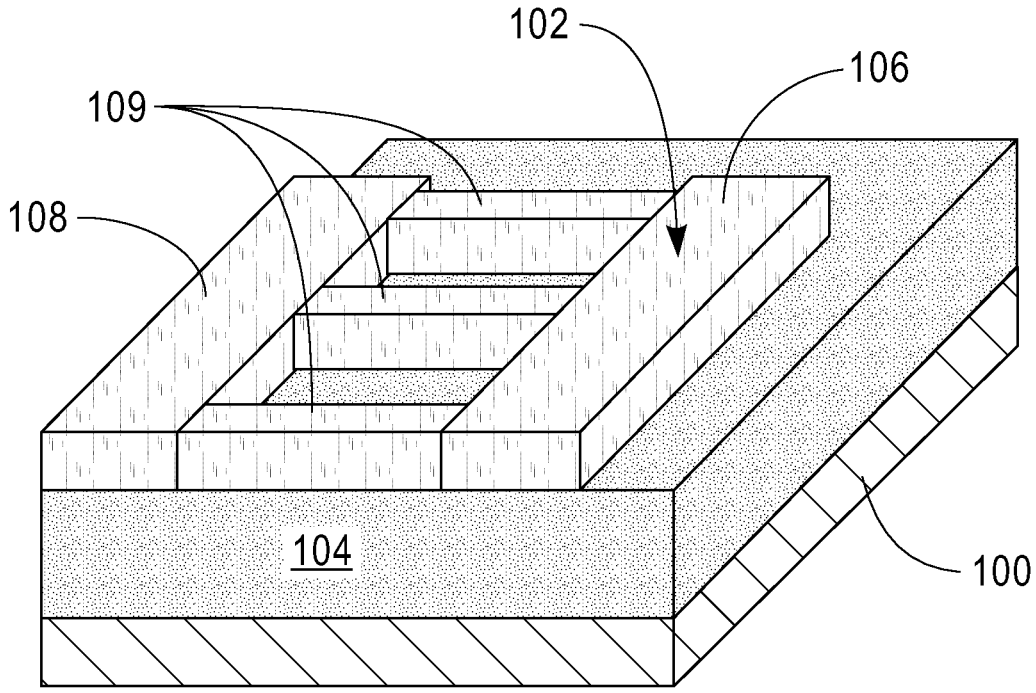
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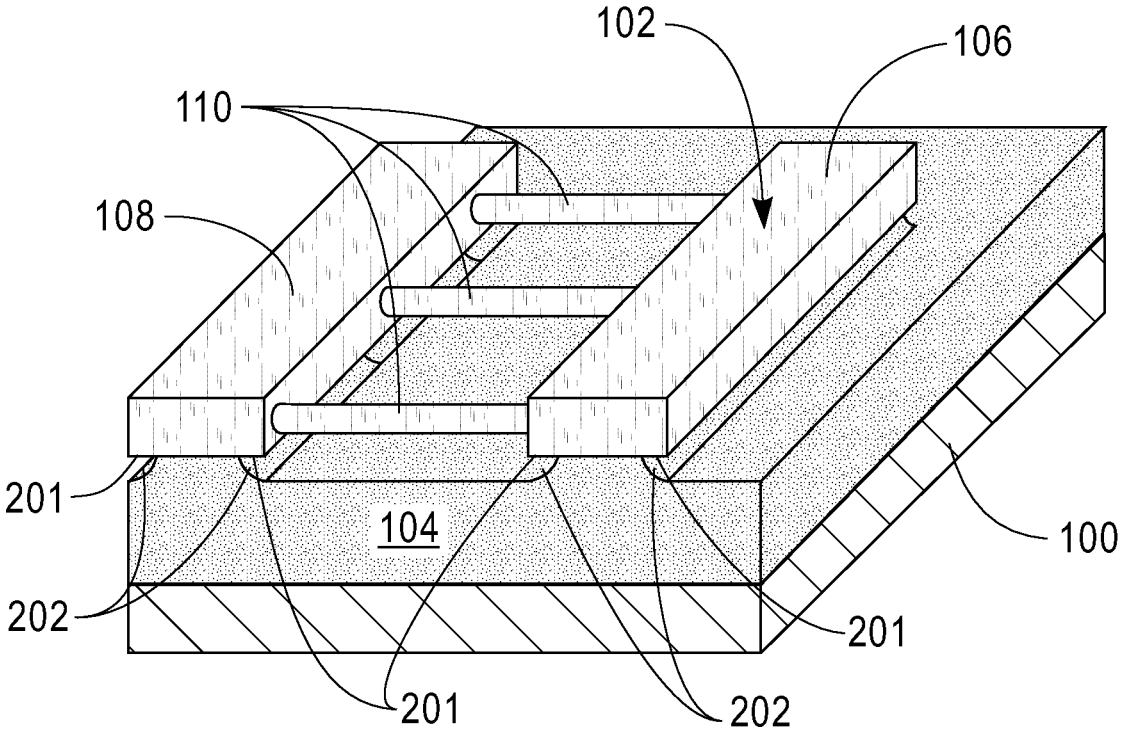
FIG. 1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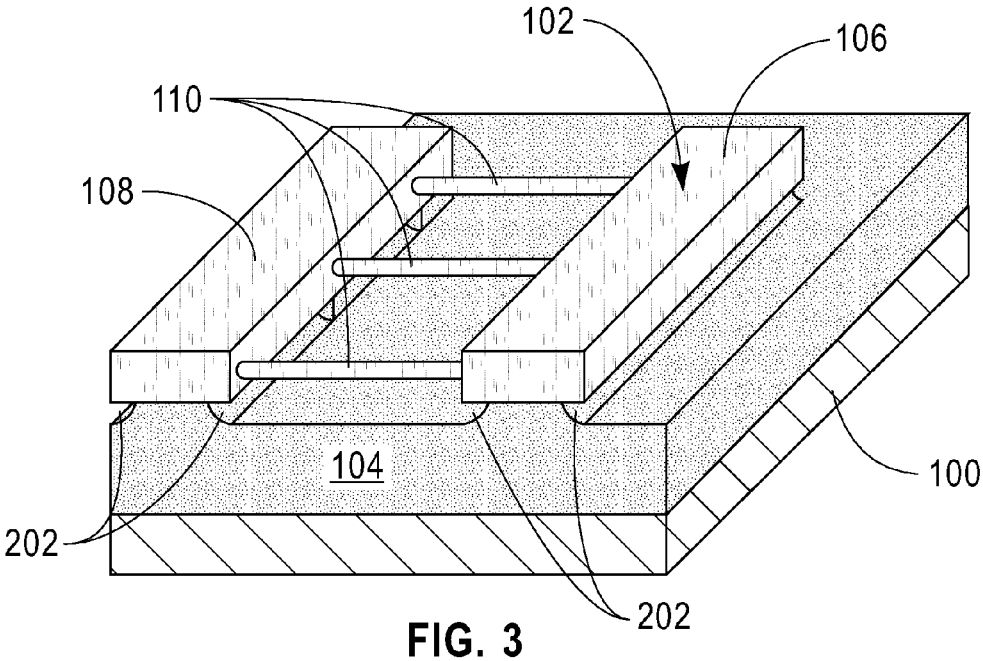
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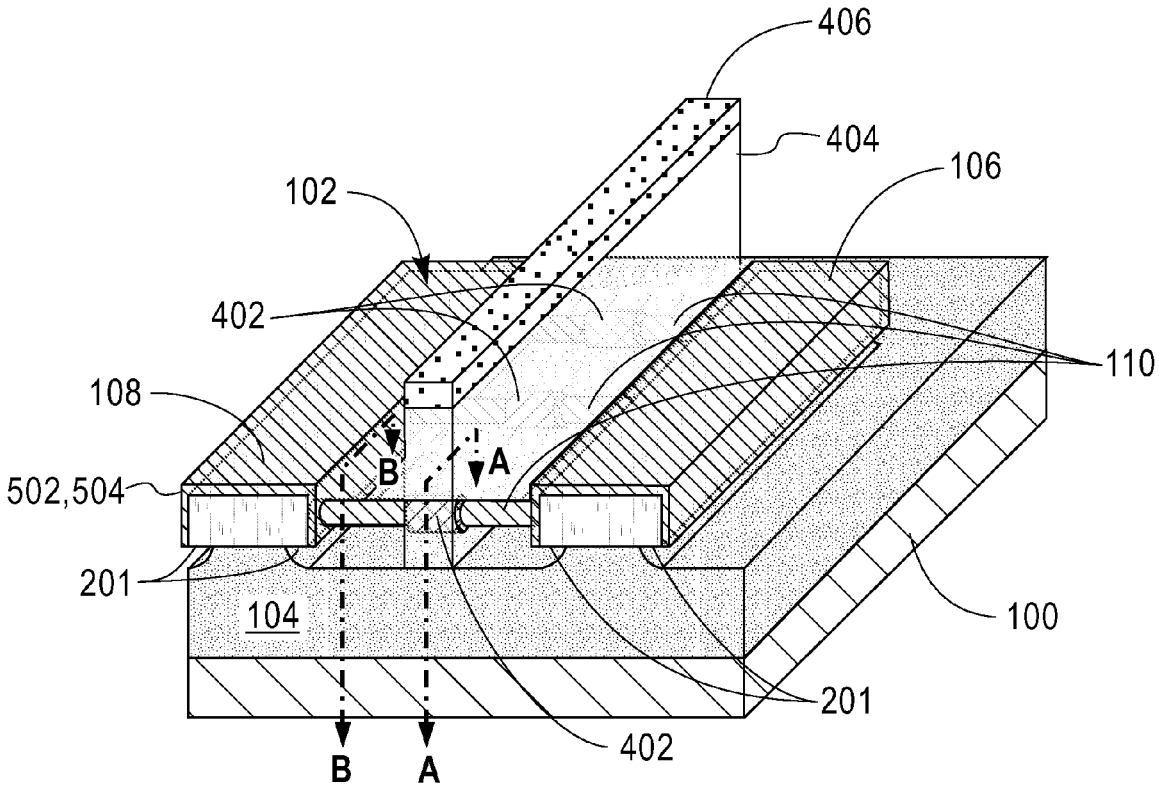
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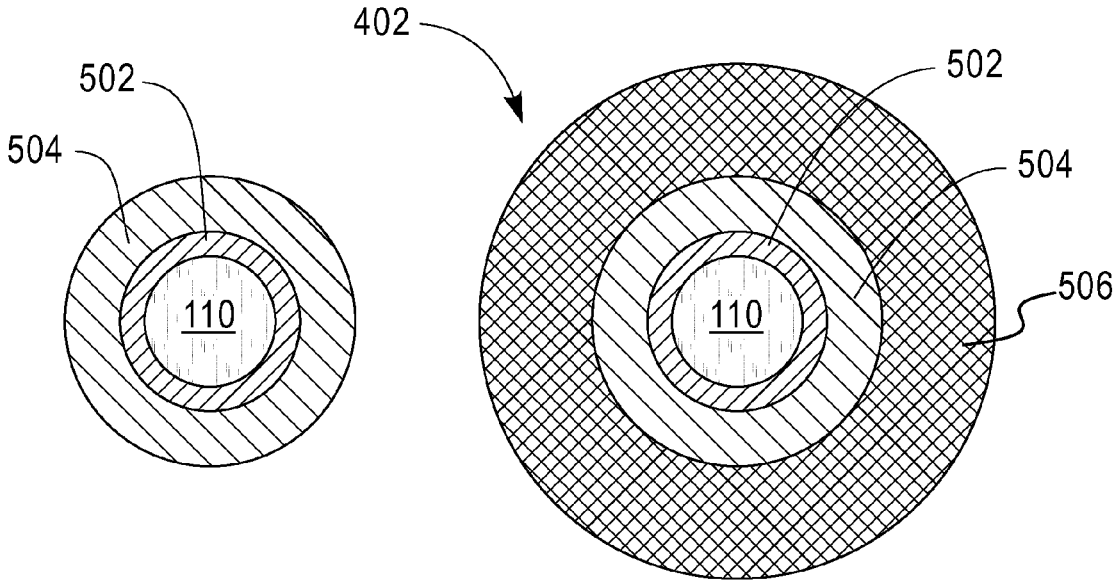
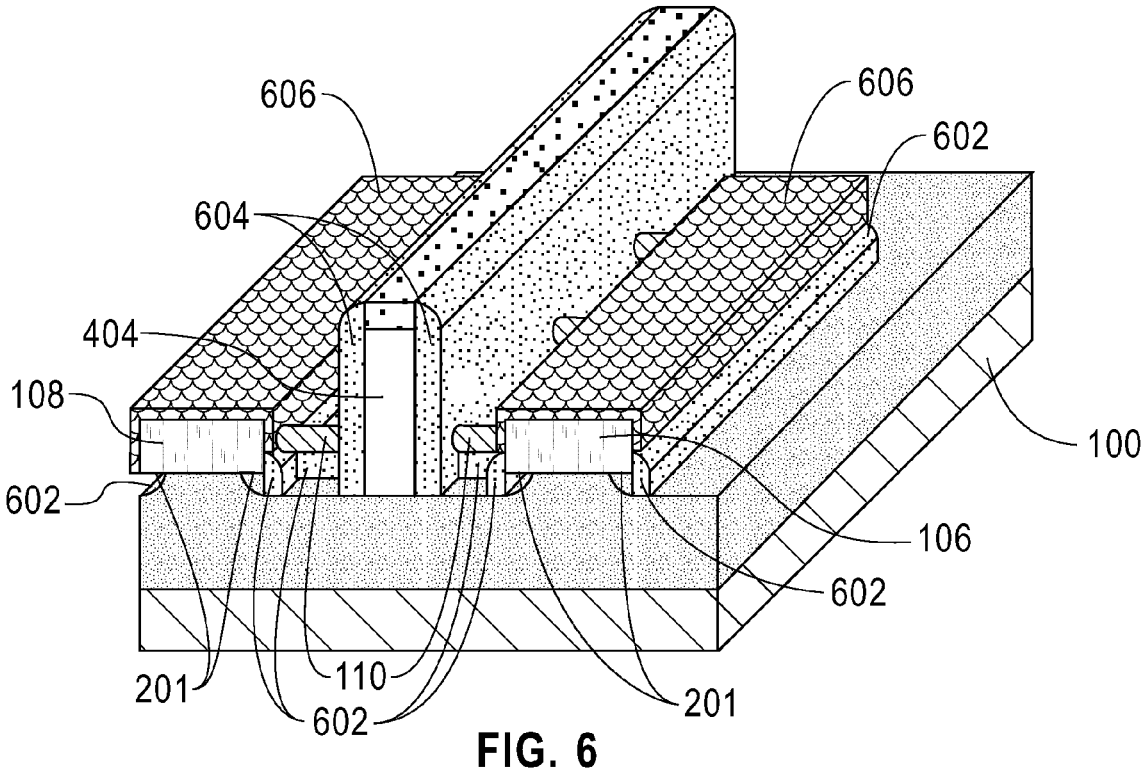


FIG. 5B FIG. 5A



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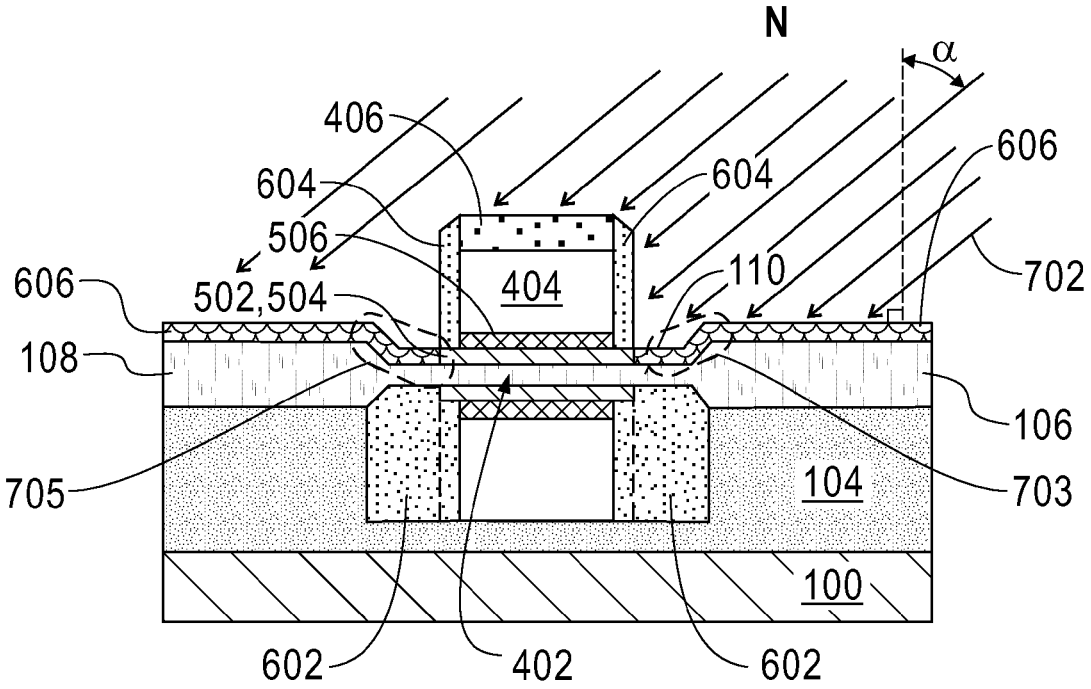
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FIG. 7

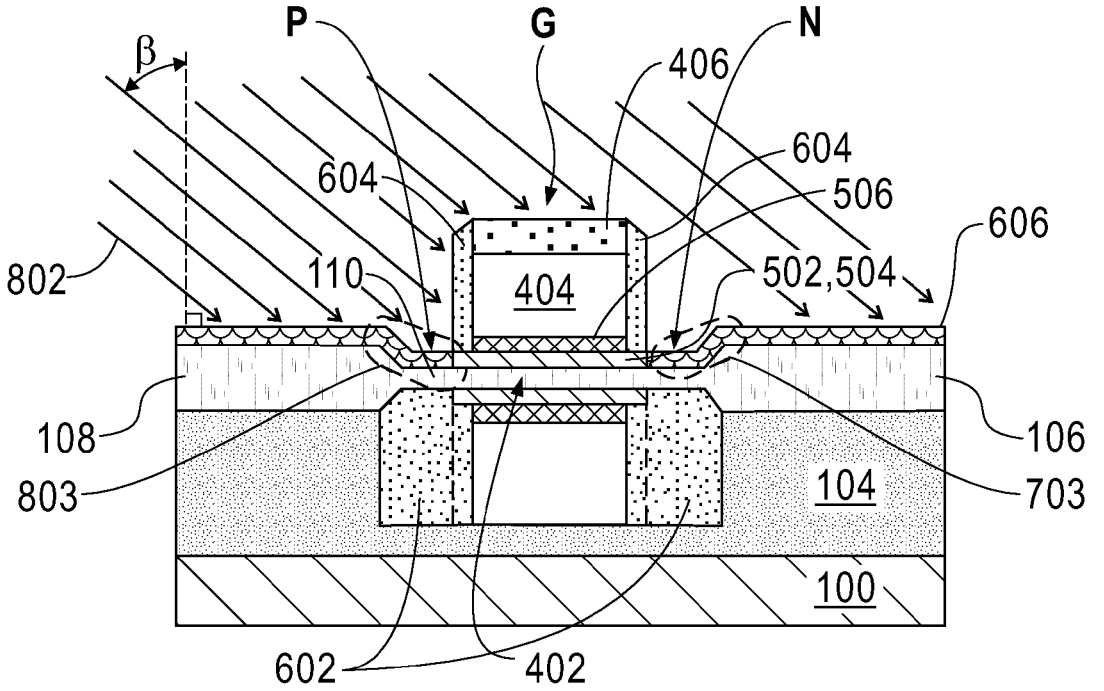
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FIG. 8

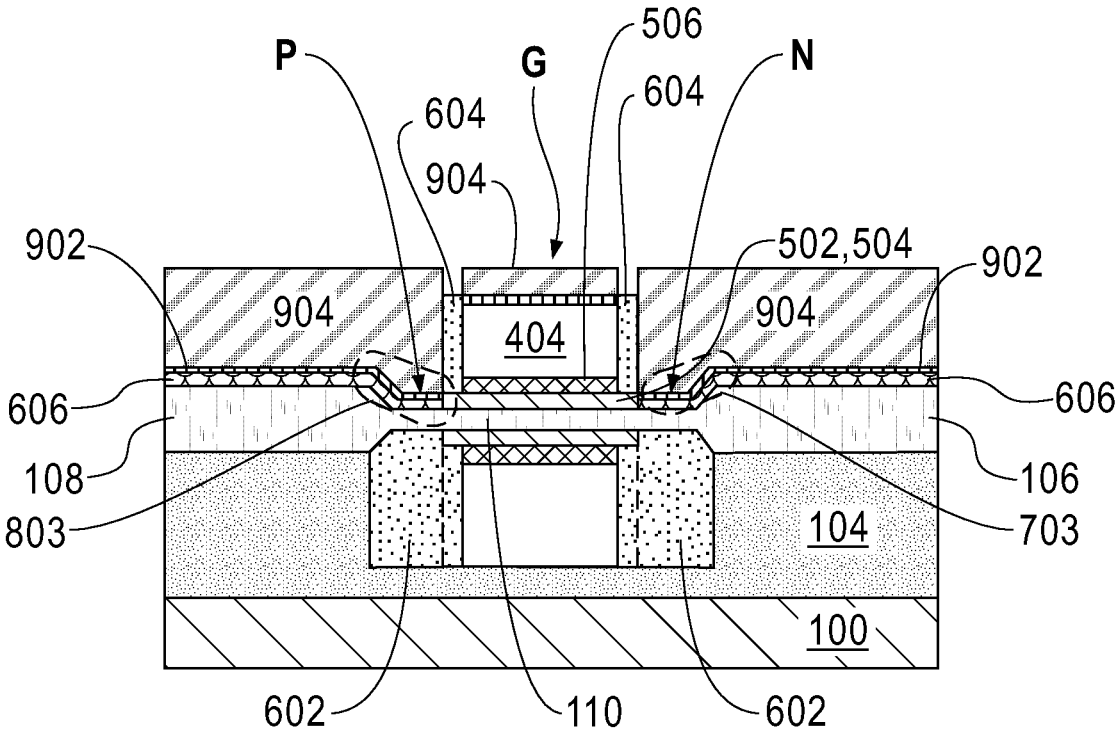
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FIG. 9

NANOWIRE PIN TUNNEL FIELD EFFECT DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Ser. No. 12/684,280, filed Jan. 8, 2010, which is incorporated by reference herein.

FIELD OF INVENTION

The present invention relates to semiconductor nanowire tunnel devices.

DESCRIPTION OF RELATED ART

PIN (p-type semiconductor—intrinsic semiconductor—n-type semiconductor) tunnel field effect transistor (FET) devices include an intrinsic semiconductor channel region disposed between a p-typed doped semiconductor region and an n-typed doped semiconductor region that contact the channel region.

BRIEF SUMMARY

In one aspect of the present invention, a method for forming a nanowire tunnel device includes forming a nanowire suspended by a first pad region and a second pad region over a semiconductor substrate, forming a gate structure around a channel region of the nanowire, implanting a first type of ions at a first oblique angle in a first portion of the nanowire and the first pad region, and implanting a second type of ions at a second oblique angle in a second portion of the nanowire and the second pad region.

In another aspect of the present invention, a nanowire tunnel device includes a nanowire suspended above a semiconductor substrate by a first pad region and a second pad region, the nanowire having a channel portion surrounded by a gate structure disposed circumferentially around the nanowire, an n-type doped region including a first portion of the nanowire adjacent to the channel portion, and a p-type doped region including a second portion of the nanowire adjacent to the channel portion.

Additional features and advantages are realized through the techniques of the present invention. Other embodiments and aspects of the invention are described in detail herein and are considered a part of the claimed invention. For a better understanding of the invention with the advantages and the features, refer to the description and to the drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The forgoing and other features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

FIGS. **1-9** illustrate an exemplary method for forming a nanowire device.

DETAILED DESCRIPTION

With reference now to FIG. **1**, a silicon on insulator (SOI) portion **102** is defined on a buried oxide (BOX) layer **104** that is disposed on a silicon substrate **100**. The SOI portion **102** includes an SOI pad region **106**, an SOI pad region **108**, and nanowire portions **109**. The SOI portion **102** may be patterned by the use of lithography followed by an etching process such as, for example, reactive ion etching (RIE).

FIG. **2** illustrates the resultant BOX layer **104** and SOI portion **102** following an isotropic etching process. The BOX layer **104** is recessed in regions not covered by SOI portion **102**. The isotropic etching results in the lateral etching of portions of the BOX layer **104** that are under the SOI portion **102**. The lateral etch suspends the nanowire portions **109** above the BOX layer **104**. The lateral etch forms the undercuts **202** in the BOX layer **104** and overhang portions **201** at the edges of SOI regions **106** and **108**. The isotropic etching of the BOX layer **104** may be, for example, performed using a diluted hydrofluoric acid (DHF). A 100:1 DHF etches about 2 to 3 nm of BOX layer **104** per minute at room temperature. Following the isotropic etching the nanowires portions **109** are smoothed to form nanowires **110** with for example, elliptical or circular cross sections that are suspended above the BOX layer **104** by the SOI pad region **106** and the SOI pad region **108**. The smoothing of the nanowires may be performed by, for example, annealing of the nanowires **109** in hydrogen. Example annealing temperatures may be in the range of 600° C.-900° C., and a hydrogen pressure of approximately 7 to 600 Torr.

FIG. **3** illustrates the nanowires **110** following an oxidation process that may be performed to reduce the cross-sectional area of the nanowires **110**. The reduction of the cross-sectional area of the nanowires **110** may be performed by, for example, an oxidation of the nanowires **110** followed by the etching of the grown oxide. The oxidation and etching process may be repeated to achieve a desired nanowire **110** cross-sectional area. Once the desired cross-sectional area of the nanowires **110** have been reached, gates are formed over the channel regions of the nanowires **110** (described below).

FIG. **4** illustrates gates **402** that are formed around the nanowires **110**, as described in further detail below, and capped with a polysilicon layer (capping layer) **404**. A hardmask layer **406**, such as, for example silicon nitride (Si_3N_4) is deposited over the polysilicon layer **404**. The polysilicon layer **404** and the hardmask layer **406** may be formed by depositing polysilicon material over the BOX layer **104** and the SOI portion **102**, depositing the hardmask material over the polysilicon material, and etching by RIE to form the polysilicon layer **404** and the hardmask layer **406**. The etching of the gate **402** may be performed by directional etching that results in straight sidewalls of the gate **402**. Following the directional etching, polysilicon **404** remains under the nanowires **110** and outside the region encapsulated by the gate **402**. Isotropic etching may be performed to remove polysilicon **404** from under the nanowires **110**.

FIG. **5**A illustrates a cross-gate **402** sectional view of a gate **402** along the line A-A (of FIG. **4**). The gate **402** is formed by depositing a first gate dielectric layer (high K layer) **502**, such as silicon dioxide (SiO_2) around the nanowire **110**, and the SOI pad regions **106** and **108**. A second gate dielectric layer (high K layer) **504** such as, for example, hafnium oxide (HfO_2) is formed around the first gate dielectric layer **502**. A metal layer **506** such as, for example, tantalum nitride (TaN) is formed around the second gate dielectric layer **504**. The metal layer **506** is surrounded by polysilicon layer **404** (of FIG. **4**A). Doping the polysilicon layer **404** with impurities such as boron (p-type), or phosphorus (n-type) makes the polysilicon layer **404** conductive. The metal layer **506** is removed by an etching process such as, for example, RIE from the nanowire **110** that is outside of the channel region

and the SOI pad regions **106** and **108**, and results in the gate **402** and nanowire **110** having the first gate dielectric layer (high K layer) **502**, around the nanowire **110** and the second gate dielectric layer (high K layer) **504** formed around the first gate dielectric layer **502**. FIG. **5**B illustrates a cross sectional view of a portion of the nanowire **110** along the line B-B (of FIG. **4**).

FIG. **6** illustrates the spacer portions **604** formed along opposing sides of the polysilicon layer **404**. The spacers are formed by depositing a blanket dielectric film such as silicon nitride and etching the dielectric film from the horizontal surfaces by RIE. The spacer walls **604** are formed around portions of the nanowire **110** that extend from the polysilicon layer **404** and surround portions of the nanowires **110**. FIG. **6** includes spacer portions **602** that are formed under the nanowires **110**, and in the undercut regions **202** (of FIG. **2**). Following the formation of the spacer portions **604**, the high K layers **502** and **504** may be removed by, for example, a selective etching process, and silicon may be epitaxially grown on the exposed nanowires **110** and SOI pad regions **106** and **108**. The epitaxially grown silicon (epi-silicon) **606** layer increases the diameter of the nanowires **110** and the dimensions of the SOI pad regions **106** and **108**. The epi-silicon **606** may be formed by epitaxially growing, for example, silicon (Si), a silicon germanium (SiGe), or germanium (Ge). As an example, a chemical vapor deposition (CVD) reactor may be used to perform the epitaxial growth. Precursors for silicon epitaxy include $SiCl_4$, SiH_4 combined with HCL. The use of chlorine allows selective deposition of silicon only on exposed silicon surfaces. A precursor for SiGe may be GeH_4, which may obtain deposition selectivity without HCL. Deposition temperatures may range from 550° C. to 1000° C. for pure silicon deposition, and as low as 300° C. for pure Ge deposition.

FIG. **7** illustrates a cross-sectional view of FIG. **6** following the formation of the spacers **604** and the epi-silicon **606**. In the illustrated embodiment, regions of the exposed epi-silicon **606** are doped with n-type ions **702** that are implanted at an angle (α), the angle α may, for example, range from 5-50 degrees. The implantation of the n-type ions **702** at the angle α exposes the SOI pad regions **106** and **108** and the nanowire **110** one side of the device to the n-type ions **702** to form an n-type doped region **703** in the epi-silicon **606** adjacent to the gate **402**, while a region **705** of the opposing side remains unexposed to the n-type ions **702** due to the height and position of the polysilicon layer **404**, the spacers **604**, and the hardmask layer **406**.

FIG. **8** illustrates a cross-sectional view of the device. In the illustrated embodiment regions of the exposed epi-silicon **606** are implanted with p-type ions **802** at an angle (β); the angle β may, for example, range from 5-50 degrees. The implantation of the ions **802** at the angle β in the epi-silicon **606** on the SOI pad regions **108** and **106** and the adjacent nanowire **110** form a p-type doped region **803** in the region **705** (of FIG. **7**) adjacent to the gate **402**; while the opposing (n-type doped region **703**) remains unexposed to the p-type ions **802**. Portions of the SOI pad regions **106** and **108** that do not include the regions **703** and **803** may include both n-type and p-type ions; the regions with both types of ions do not appreciably effect the operation of the device.

Once the ions **702** and **802** are implanted, an annealing process is performed to overlap the device and activate the dopants. The annealing process results in a shallow doping gradient of n-type ions and p-type ions in the channel region of the device.

FIG. **9** illustrates the resultant structure following silicidation where a silicide **902** is formed on the over the polysilicon layer **404** (the gate region G) and over the n-type doped region (N) **703** and the p-typed doped region (P) **803**. Examples of silicide forming metals include Ni, Pt, Co, and alloys such as NiPt. When Ni is used the NiSi phase is formed due to its low resistivity. For example, formation temperatures include 400-600° C. Once the silicidation process is performed, capping layers and vias for connectivity (not shown) may be formed and a conductive material such as, Al, Au, Cu, or Ag may be deposited to form contacts **904**.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one ore more other features, integers, steps, operations, element components, and/or groups thereof.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated

The diagrams depicted herein are just one example. There may be many variations to this diagram or the steps (or operations) described therein without departing from the spirit of the invention. For instance, the steps may be performed in a differing order or steps may be added, deleted or modified. All of these variations are considered a part of the claimed invention.

While the preferred embodiment to the invention had been described, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the invention first described.

What is claimed is:

1. A nanowire tunnel device, comprising:

a nanowire spaced apart and above a semiconductor substrate by a first pad region and a second pad region, the nanowire having a channel portion surrounded by a gate structure disposed circumferentially around the nanowire, the gate structure comprising a metal layer and a conductive polysilicon capping layer disposed directly onto and encapsulating the metal layer;

a first protective spacer adjacent to a sidewall of the gate structure and around portions of the nanowire extending from the gate structure;

a second protective spacer adjacent to the first protective spacer, the second protective spacer is formed and fills a space between an exposed region of the nanowire and the semiconductor substrate;

an n-type doped region including a first portion of the nanowire adjacent to the channel portion; and

a p-type doped region including a second portion of the nanowire adjacent to the channel portion.

2. The device of claim **1**, wherein the gate structure includes a silicon oxide layer disposed on the channel portion of the nanowire, a dielectric layer disposed on the silicon oxide layer, and a metal layer disposed on the dielectric layer.

3. The device of claim **1**, wherein the first portion of the nanowire, the second portion of the nanowire, the first pad region, and the second pad region include silicon material.

4. The device of claim **1**, wherein the first portion of the nanowire, the second portion of the nanowire, the first pad region, and the second pad region include epitaxially grown material.

5. The device of claim **4**, wherein the epitaxially grown material is silicon.

6. The device of claim **4**, wherein the epitaxially grown material is a SiGe alloy.

7. The device of claim **4**, wherein the epitaxially grown material is Ge.

8. The device of claim **4**, wherein the epitaxially grown material is doped silicon.

9. The device of claim **4**, wherein the epitaxially grown material is a doped SiGe alloy.

10. The device of claim **4**, wherein the epitaxially grown material is doped Ge.

11. The device of claim **1**, wherein further comprising a silicide material on the first pad region, the second pad region, the first portion of the nanowire, the second portion of the nanowire, and the gate structure.

12. The device of claim **1**, further comprising conductive contacts on the first pad region, the second pad region, the first portion of the nanowire, the second portion of the nanowire, and the gate structure.

13. The device of claim **1**, wherein the first protective spacer includes a nitride material.

14. The device of claim **1**, wherein the conductive polysilicon capping layer is doped with p-type or n-type impurities.

15. The device of claim **1**, further comprising a hard mask layer disposed onto the conductive polysilicon capping layer.

16. A nanowire tunnel device, comprising:

a nanowire spaced apart and above a semiconductor substrate by a first pad region and a second pad region, the nanowire having a channel portion surrounded by a gate structure disposed circumferentially around the nanowire, the gate structure comprising a metal layer and a conductive polysilicon capping layer disposed directly onto and encapsulating the metal layer;

a first protective spacer adjacent to a sidewall of the gate structure and around portions of the nanowire extending from the gate structure;

a second protective spacer adjacent to the first protective spacer, the second protective spacer is formed and fills a space between an exposed region of the nanowire and the semiconductor substrate;

an n-type doped region including a first portion of the nanowire adjacent to the channel portion; and

a p-type doped region including a second portion of the nanowire adjacent to the channel portion, wherein the first portion of the nanowire, the second portion of the nanowire, the first pad region, and the second pad region include epitaxially grown material.

17. The device of claim **16**, wherein the gate structure includes a silicon oxide layer disposed on the channel portion of the nanowire, a dielectric layer disposed on the silicon oxide layer, and a metal layer disposed on the dielectric layer.

18. The device of claim **16**, wherein the first portion of the nanowire, the second portion of the nanowire, the first pad region, and the second pad region include silicon material.

19. The device of claim **16**, wherein the epitaxially grown material is Ge.

20. A nanowire tunnel device, comprising:

a nanowire spaced apart and above a semiconductor substrate by a first pad region and a second pad region, the nanowire having a channel portion surrounded by a gate structure disposed circumferentially around the nanowire, the gate structure comprising a metal layer, a conductive polysilicon capping layer disposed directly onto and encapsulating the metal layer, and a silicon nitride hardmask layer disposed directly onto the polysilicon capping layer;

a first protective spacer adjacent to a sidewall of the gate structure and around portions of the nanowire extending from the gate structure;

a second protective spacer adjacent to the first protective spacer, the second protective spacer is formed and fills a space between an exposed region of the nanowire and the semiconductor substrate;

an n-type doped region including a first portion of the nanowire adjacent to the channel portion; and

a p-type doped region including a second portion of the nanowire adjacent to the channel portion.

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